Verification

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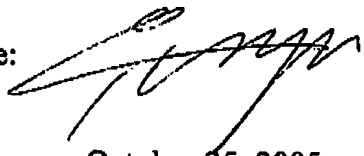
Signature: 

Date: October 25, 2005

Name: Chan-Joo YOUN

KOREAN INDUSTRIAL

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Date of Application : **November 08, 2002**

Applicant(s) : **LG. Philips LCD Co., Ltd.**

COMMISSIONER

[BIBLIOGRPHICAL DOCUMENTS]

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[CLSSIFICATION] PATENT

[RECIPIENT] COMMISSIONER

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[TITLE OF INVENTION IN KOREAN] 액정표시장치용 어레이기판의 제조방법

[TITLE OF INVENTION IN ENGLISH] Method for fabricating of an array substrate for LCD

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[PURPORT] We submit application as above under the article 42 of the Patent Law.

Attorney Jung, Won-Ki (seal)

[FEES]

[BASIC APPLICATION FEE]	20 pages	29,000	won
[ADDITIONAL APPLICATION FEE]	5 pages	5,000	won
[PRIORITY FEE]	0 things	0	won
[EXAMINATION REQUEST FEE]	0 clamis	0	Won
[TOTAL]		34,000	Won

[ENCLOSED] 1. Abstract, Specifications (with Drawings)_1 set

[DOCUMENT OF ABSTRACT]

[ABSTRACT]

The present invention relates to a liquid crystal display device, and more particularly, to a method of forming a metal line on an array substrate for a liquid crystal display device.

In the present invention, a metal line such as a gate line and a data line on an array substrate for a liquid crystal display device is formed of a double-layered metal patterns including copper/molybdenum alloy (Cu/Mo-alloy).

Since adhesion of the Cu layer to the substrate is improved due to the Mo-alloy layer, lift of the metal line is prevented. In addition, the substrate does not have any surface damage from an etching solution during an etching process of the metal line. Moreover, since the Mo-alloy layer is more chemically resistive than a Mo layer, an over-etch phenomenon under the Cu layer is prevented, stain of image due to scratch of the substrate is prevented and the liquid crystal display device can have an improved picture quality. Further, a production yield is improved because lift of lines is prevented.

[REPRESENTATIVE FIGURE]

FIG. 10e

[SPECIFICATIONS]

[NAME OF INVENTION]

Method for fabricating of an array substrate for LCD

[BRIEF EXPLANATION OF FIGURES]

FIG. 1 is a schematic view showing a liquid crystal display device according to the related art,

FIG. 2 is a schematic cross-sectional view taken along a line II-II' of FIG. 1,

FIGs. 3 and 4 are enlarged plane and cross-sectional photographs of partially-etched copper/titanium (Cu/Ti) double layers taken by the SEM (Scanning Electron Microscope),

FIGs. 5 and 6 are enlarged plane and cross-sectional photographs of partially-etched copper/molybdenum (Cu/Mo) double layers taken by the SEM (Scanning Electron Microscope),

FIGs. 7 and 8 are enlarged plane and cross-sectional photographs of partially-etched copper/molybdenum-alloy (Cu/Mo-alloy) double layers according to the present invention taken by the SEM (Scanning Electron Microscope),

FIG. 9 is a partially enlarged plane view of an array substrate for a liquid crystal display device according to the present invention, and

FIGs. 10a to 10e are cross-sectional views taken along a line IX-IX' of FIG. 9 and illustrating fabrication process of an array substrate according to the present invention.

* Explanation of major parts in the figures *

200 : substrate
202 : gate line
204 : gate electrode
206 : gate insulating layer
208 : active layer
210 : ohmic contact layer
212 : data line
214 : source electrode
216 : drain electrode
218 : metal layer of island shape
220 : passivation layer
222 : pixel electrode

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display device, and more particularly, to a method of forming a metal line on an array substrate for a liquid crystal display device.

Hereinafter, reference will now be made in detail to a liquid crystal display device according to the related art, example of which is illustrated in the accompanying drawings.

FIG. 1 is a schematic view of a liquid crystal display device according to the related art.

As shown in FIG. 1, the liquid crystal display (LCD) device 11 includes an upper substrate 5, referred to as a color filter substrate, and a lower substrate 10, referred to as an array substrate, having a liquid crystal layer 9 interposed therebetween. On the upper substrate 5, a black matrix 6, and a color filter layer 7 are formed in a shape of an array matrix including a plurality of red (R), green (G), and blue (B) color filters surrounded by the black matrix 6. Additionally, a common electrode 18 is formed on the upper substrate 5 to cover the color filter layer 7 and the black matrix 6.

On the lower substrate 10, a plurality of thin film transistors T are formed in a shape of an array matrix corresponding to the color filter layer 7. A plurality of crossing gate lines 14

and data lines 22 are perpendicularly positioned such that each TFT T is located adjacent to each intersection of the gate lines 14 and the data lines 22.

Furthermore, a plurality of pixel electrodes 17 are formed on a pixel region P defined by the gate lines 14 and the data lines 22 of the lower substrate 10.

The pixel electrode 17 includes a transparent conductive material having high transmittance, such as indium-tin-oxide (ITO) or indium-zinc-oxide (IZO).

Although not shown in FIG. 1, the LCD device 11 includes a backlight under the lower substrate 10. The backlight (not shown) irradiates light towards the lower and upper substrates 10 and 5.

In the related art LCD device shown in FIG. 1, a scanning signal is applied to a gate electrode of the thin film transistor T through the gate line 14, and a data signal is applied to a source electrode of the thin film transistor T through the data line 22.

As a result, the liquid crystal molecules of the liquid crystal layer 9 are re-aligned and re-arranged by operation of the thin film transistor T, and incident light from the backlight (not shown) passing through the liquid crystal layer 9 is controlled to display an image.

Namely, the electric fields induced between the pixel and common electrodes 17 and 18 re-arrange the liquid crystal molecules of the liquid crystal layer 9 so that the incident light can be converted into the desired images in accordance with the induced electric fields.

There are various factors that affect and define a picture quality of the LCD device 11. Among those various factors, electric resistance of the gate and data lines 14 and 22 is an important requisition for achieving the improved picture quality in the LCD device 11.

As the gate and data lines 14 and 22 have the lower electrical resistance, the signal delay becomes reduced in those lines and thus the picture quality can become improved.

For the purposed of obtaining the reduced signal delay, copper (Cu) having relatively low electric resistance is used for the gate and data lines 14 and 22. However, since the copper (Cu) does not have a good adhesion to the substrate, a buffer metal layer, for example, titanium (Ti) or molybdenum (Mo), is used between the substrate and the copper (Cu).

Hereinafter, a cross-sectional structure of a pixel region of an array substrate will be illustrated with reference to FIG. 2.

FIG. 2 is a cross-sectional view taken along line II-II' of FIG. 1 and illustrating a pixel of a related art array substrate.

As shown in FIG. 2, the gate line 14 and the data line 22 crossing each other to define the pixel region P are formed on the lower substrate 10, and the thin film transistor T is formed near the crossing of the gate line 14 and the data line 22. The thin film transistor T includes a gate electrode 30, an active layer 34, an ohmic contact layer 36, a source electrode 38, and a drain electrode 40. The pixel electrode 17 connected to the drain electrode 40 is formed in the pixel region P.

The gate line 14 and the gate electrode 30 are formed of the same material and the same layer, and the data line 22 and the source and the drain electrodes 38 and 40 are formed of the same material and the same layer.

Between the gate electrode 30 and the active layer 34, a gate insulating layer 32 is interposed to protect the gate electrode 30 and the gate line 14.

In the related art array substrate, one of the gate electrode 30 and the source and drain electrodes 38 and 40 has a double-layered structure having copper/titanium (Cu/Ti) layers or copper/molybdenum (Cu/Mo) layers.

Generally, OXONE (2KHSO5·KHSO4·K2SO4) is used as a solution for etching the Cu layer of the double-layered structure, and a mixture solution of OXONE, hydrogen

fluoride (HF) and ammonium fluoride (NH4F) is used as a solution for etching the Ti layer of the double-layered structure.

When etching the copper/titanium (Cu/Ti) layers using the a mixture solution of OXONE, hydrogen fluoride (HF) and ammonium fluoride (NH4F) to form the gate line and electrode, the mixture solution damages and unevenly etches the surface of the substrate due to the fact that the F– ions is contained in the mixture solution. The damages and uneven etch of the substrate surface cause the decreased degree of image quality in the liquid crystal display device, such as generation of stained and spotted images.

Furthermore, when the copper/titanium (Cu/Ti) layers are applied for the data line, the source electrode and the drain electrode, the underlying gate insulating layer is definitely etched and damaged by the etchant. Therefore, the damages and uneven etch of the gate insulating layer also cause the decreased degree of image quality in the liquid crystal display device.

FIGs. 3 and 4 are enlarged plane and cross-sectional photographs of partially-etched copper/titanium (Cu/Ti) double layers taken by the SEM (Scanning Electron Microscope).

As indicated in FIG. 3, the substrate 50 has an irregularly etched and damaged surface.

Especially in FIG. 4, a titanium (Ti) layer 52a is first formed on a substrate 50 and a copper (Cu) layer 52b is then formed on the titanium (Ti) layer. It is much more noticeable that the surface of substrate 50 is severely.

Particularly, the substrate 50 of glass is etched as much as about 400 angstroms (Å) from its primary surface.

Meanwhile, when using the copper/molybdenum (Cu/Mo) layers for the double-layered metal patterns, the underlying molybdenum (Mo) layer is damaged and the copper (Cu) layer is undercut by the damaged molybdenum (Mo) layer although the glass substrate is

not damaged. Since the etchant for the copper/molybdenum (Cu/Mo) layers damages the Mo layer, the Cu layer is lifted off from the substrate.

FIGs. 5 and 6 are enlarged plane and cross-sectional photographs of partially-etched copper/molybdenum (Cu/Mo) double layers taken by the SEM (Scanning Electron Microscope).

As shown in FIG. 5, a surface of the substrate 50 is not damaged and has a flat top surface.

However, as indicated in FIG. 6, the Mo layer 60b under the Cu layer 60a is over-etched inwardly and damaged at a portion A.

As shown in FIGs. 3 to 6, in case of Cu/Ti layers, the substrate of glass is damaged by a solution for etching the Cu/Ti layers. In case of Cu/Mo layers, the Mo layer is over-etched by a solution for etching the Cu/Mo layers and the Cu layer is lifted off from the substrate.

[TECHNICAL SUBJECT OF INVENTION]

To solve the above problems, an object of the present invention is to provide an array substrate for a liquid crystal display device where a gate line and a data line include a double-layered metal pattern of copper/mol molybdenum alloy (Cu/Mo-alloy) layers.

Since molybdenum alloy has a strong chemical resistance, the Mo-alloy layer is not over-etched and the substrate is not damaged.

Accordingly, operation characteristics and display deterioration of a liquid crystal display device are improved, thereby obtaining a high quality liquid crystal display device.

[CONSTRUCTION AND OPERATION OF INVENTION]

To achieve these and other objects and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for a liquid crystal display device includes: a gate electrode and a gate line having a molybdenum-alloy (Mo-alloy) layer and a copper (Cu) layer sequentially on a substrate; an active layer and an ohmic contact layer on a gate insulating layer over the gate electrode; a source electrode on the ohmic contact layer, a drain electrode spaced apart from the source electrode, and a data line connected to the source electrode, the data line crossing the gate line to define a pixel region; a passivation layer on the source electrode, the drain electrode and the data line, the passivation layer exposing a portion of the drain electrode; and a transparent pixel electrode in the pixel region, the pixel electrode contacting the drain electrode.

The source electrode, the drain electrode and the data line include one of copper (Cu) and copper/molly-alloy (Cu/Mo-alloy).

In another aspect of the present, a method of fabricating an array substrate for a liquid crystal display device includes: forming a gate line and a gate electrode connected to the gate line by sequentially depositing and pattering molybdenum-alloy (Mo-alloy) layer and a copper (Cu) layer on a substrate; forming a gate insulating layer over the substrate having the gate line and the gate electrode; forming an active layer and an ohmic contact layer sequentially on the gate insulation layer over the gate electrode; forming a data line, a source electrode and a drain electrode, the data line perpendicularly crossing the gate line to define a pixel region, the source electrode and the drain electrode spaced apart from each other on the ohmic contact layer; forming a passivation layer over the substrate having the source and drain electrodes, the passivation layer exposing a portion of the drain electrode; and forming a pixel electrode in the pixel region, the pixel electrode contacting the drain electrode.

The passivation layer includes one of an inorganic insulating material having silicon nitride (SiNx) and silicon oxide (SiO2), and an organic insulating material having benzocyclobutene (BCB) and acrylic resin.

The data line, the source electrode, the drain electrode include one of copper (Cu) layer and copper/molly-alloy (Cu/Mo-alloy).

The molybdenum alloy (Mo-alloy) layer includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

Hereinafter, reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

-- EMBODIMENT --

In an array substrate for a liquid crystal display device according to the present invention, a gate line and a data line are formed of a copper/molybdenum-alloy (Cu/Mo-alloy) layers.

FIGs. 7 and 8 are enlarged plane and cross-sectional photographs of partially-etched copper/molybdenum-alloy (Cu/Mo-alloy) double layers taken by the SEM (Scanning Electron Microscope),

As shown in FIG. 7, a molybdenum-alloy (Mo-alloy) layer 102 is first formed on a substrate 100 and then a copper (Cu) layer 104 is sequentially formed on the molybdenum alloy (Mo-alloy) layer 102. Thereafter, the Mo-alloy layer 102 and the Cu layer 104 are patterned to form a Cu/Mo-alloy double-layered metal pattern. After patterning, a surface of the substrate 100 is smooth as indicated in FIG. 7.

The Mo-alloy layer 102 is 10 to 500 angstroms (Å) in thickness, and the Cu layer 104 is 500 to 5000 angstroms(Å) in thickness.

Especially in FIG. 8, the patterned Mo-alloy layer 102 is formed on the substrate 100 and then the pattern Cu layer 104 is formed on the Mo-alloy layer 102. Unlike the related arts, the substrate 100 is not unevenly etched and damaged. Furthermore, the Mo-alloy layer 102 is not also damaged and corroded under the Cu layer 104. Namely, the Mo-alloy layer 102 and the Cu layer 104 are properly etched to have a taper shape B.

Accordingly, it is clear that if the Mo-alloy layer is used as a buffer metal layer under the Cu layer, a solution for etching the Cu/Mo-alloy layers does not hurt the substrate and the underlying Mo-alloy layer.

In the present invention, the molybdenum alloy (Mo-alloy) includes tungsten (W), neodymium (Nd), niobium (Nb) or the combination thereof.

FIG. 9 is a partially enlarged plane view of an array substrate for a liquid crystal display device according to the present invention, and

As shown in FIG. 9, a plurality of gate lines 202 disposed in a transverse direction and a plurality of data lines 212 disposed in a longitudinal direction on a substrate 200. The plurality of gate lines 202 and the plurality of data lines 212 cross one another to define a pixel region P.

A thin film transistor T is formed at the crossing of the gate line 202 and the data line 212. The thin film transistor T includes a gate electrode 204, an active layer 208, a source electrode 214, and a drain electrode 216.

In the pixel region P, a pixel electrode 226 is located with contacting the drain electrode 216. A storage capacitor C is formed over a portion of the gate line 202.

A first storage electrode of the storage capacitor C is the portion of the gate line 202 and a second electrode of the storage capacitor C is a metal layer 218 of an island shape contacting the pixel electrode 226.

Here in the present invention, the gate lines 202 and the data lines 212 are formed of Cu/Mo-alloy layers. Alternatively, the data line 212 can be formed of a single layer of copper (Cu).

FIGs. 10a to 10e are cross-sectional views taken along a line IX-IX' of FIG. 9 and illustrating fabrication process of an array substrate according to the present invention.

In FIG. 10a, molybdenum-alloy (Mo-alloy) layer and copper (Cu) layer are sequentially formed on a substrate 200. Thereafter, the Cu/Mo-alloy layers are simultaneously patterned to form a gate line 202 and a gate electrode 204 connected to the gate line 202 on the substrate 200.

The molybdenum alloy (Mo-alloy) layer has a thickness ranging from about 10 to about 500 angstroms (Å), and the copper (Cu) layer has a thickness ranging from 500 to 5000 angstroms (Å). Beneficially, the first metal layer of molybdenum alloy (Mo-alloy) is 100 angstroms (Å), and the second metal layer of copper (Cu) is 2000 angstroms (Å).

Thereafter, a gate insulating layer 206 (or a first insulating layer) is formed on the substrate 200 to cover the gate line 202 and the gate electrode 204. The gate insulating layer 206 is formed of an inorganic material including silicon nitride (SiNx) and silicon oxide (SiO2).

In FIG. 10b, an intrinsic amorphous silicon layer (a-Si:H) and then an p+ or n+-doped amorphous silicon layer (p+a-Si:H or n+a-Si:H) are sequentially deposited on the entire surface of the gate insulating layer 206 and then simultaneously patterned to form both an

active layer 208 and an ohmic contact layer 210 on the gate insulating layer 206, especially over the gate electrode 204.

Next, in FIG. 10c, a molybdenum-alloy (Mo-alloy) layer and a copper (Cu) layer are sequentially formed over an entire of the substrate 200 to cover the active and ohmic contact layers 208 and 210. Thereafter, those metal layers are patterned to form a data line 212 crossing the gate line 202 to define a pixel region P, a source electrode 214 extending from the data line 212 toward the gate electrode 204, a drain electrode 216 spaced apart from the source electrode 214.

Simultaneously, a metal layer 218 of an island shape is formed over a portion of the gate line 202 defining the pixel region P.

Meanwhile, the data line 212 can be formed of a single layer of copper (Cu) instead of the Cu/Mo-alloy layers.

The Mo-alloy layer has good contact characteristics with the silicon of the active and ohmic contact layers 208 and 210, and prevents diffusion of silicon ions into the copper layer.

FIG. 10d, a passivation layer 220 is formed over the entire surface of the substrate 200 to cover the data line 212, the source electrode 214 and the drain electrode 216. The passivation layer 220 may be formed of an inorganic material including one of silicon nitride (SiNx) and silicon oxide (SiO2), or an organic material including one of benzocyclobutene (BCB) and acrylic resin.

Thereafter, the passivation layer 220 is patterned to form a drain contact hole 222 and a storage contact hole 224. The drain contact hole 222 exposes a portion of the drain electrode 216 and the storage contact hole 224 exposes a portion of the storage metal layer 218.

As shown in FIG. 10e, a transparent conductive metallic material including indium tin oxide (ITO) and indium zinc oxide (IZO) is deposited on the passivation layer 220 and then patterned to form a pixel electrode 226 in the pixel region. The pixel electrode 226 contacts both the drain electrode 216 and the storage metal layer 218.

Therefore, the array substrate of the present invention is complete.

[EFFECT OF INVENTION]

When a gate line and a data line are formed of Cu/Mo-alloy layers according to the present invention, a substrate or a gate insulating layer do not have any surface damages. Accordingly, a production yield is improved.

Moreover, since a copper layer having a low electric resistance is used for gate and data lines due to Cu/Mo-alloy layers, a liquid crystal display device having a high display quality can be obtained.

[RANGE OF CLAIMS]

[CLAIM 1]

An array substrate for a liquid crystal display device, comprising:

a gate electrode and a gate line having a molybdenum-alloy (Mo-alloy) layer and a copper (Cu) layer sequentially on a substrate;

an active layer and an ohmic contact layer on a gate insulating layer over the gate electrode;

a source electrode on the ohmic contact layer, a drain electrode spaced apart from the source electrode, and a data line connected to the source electrode, the data line crossing the gate line to define a pixel region;

a passivation layer on the source electrode, the drain electrode and the data line, the passivation layer exposing a portion of the drain electrode; and

a transparent pixel electrode in the pixel region, the pixel electrode contacting the drain electrode.

[CLAIM 2]

The array substrate according to claim 1, wherein the source electrode, the drain electrode and the data line include one of copper (Cu) and copper/molly-alloy (Cu/Mo-alloy).

[CLAIM 3]

A method of fabricating an array substrate for a liquid crystal display device, comprising:

forming a gate line and a gate electrode connected to the gate line by sequentially depositing and pattering molybdenum-alloy (Mo-alloy) layer and a copper (Cu) layer on a substrate;

forming a gate insulating layer over the substrate having the gate line and the gate electrode;

forming an active layer and an ohmic contact layer sequentially on the gate insulation layer over the gate electrode;

forming a data line, a source electrode and a drain electrode, the data line perpendicularly crossing the gate line to define a pixel region, the source electrode and the drain electrode spaced apart from each other on the ohmic contact layer;

forming a passivation layer over the substrate having the source and drain electrodes, the passivation layer exposing a portion of the drain electrode; and

forming a pixel electrode in the pixel region, the pixel electrode contacting the drain electrode.

[CLAIM 4]

The method according to claim 3, wherein the passivation layer includes one of an inorganic insulating material having silicon nitride (SiNx) and silicon oxide (SiO_2), and an organic insulating material having benzocyclobutene (BCB) and acrylic resin.

[CLAIM 5]

The method according to claim 3, wherein the data line, the source electrode, the drain electrode include one of copper (Cu) layer and copper/molly-alloy (Cu/Mo-alloy).

[CLAIM 6]

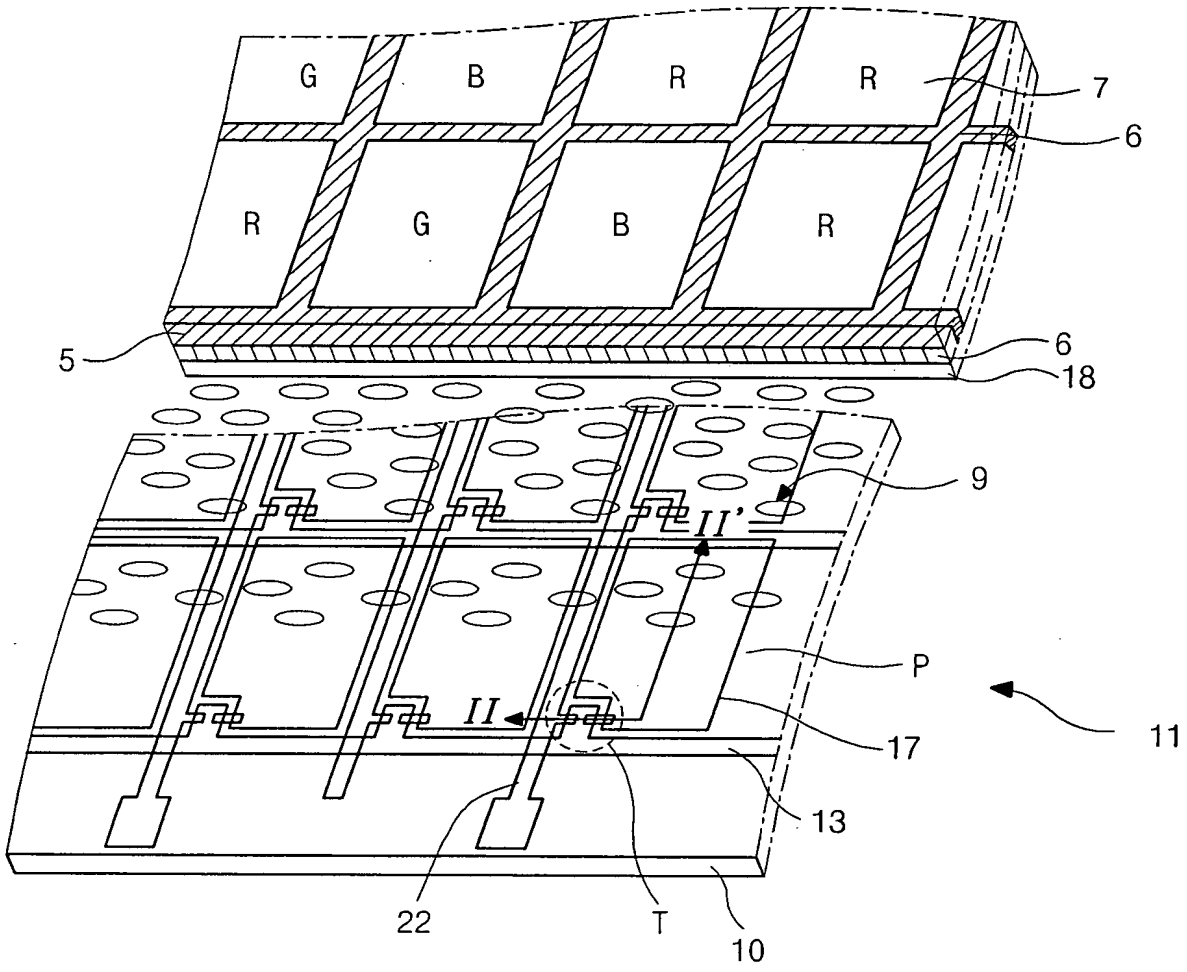
The method according to claim 3, wherein the molybdenum alloy (Mo-alloy) layer includes one of tungsten (W), neodymium (Nd), niobium (Nb) and the combination thereof.

[CLAIM 7]

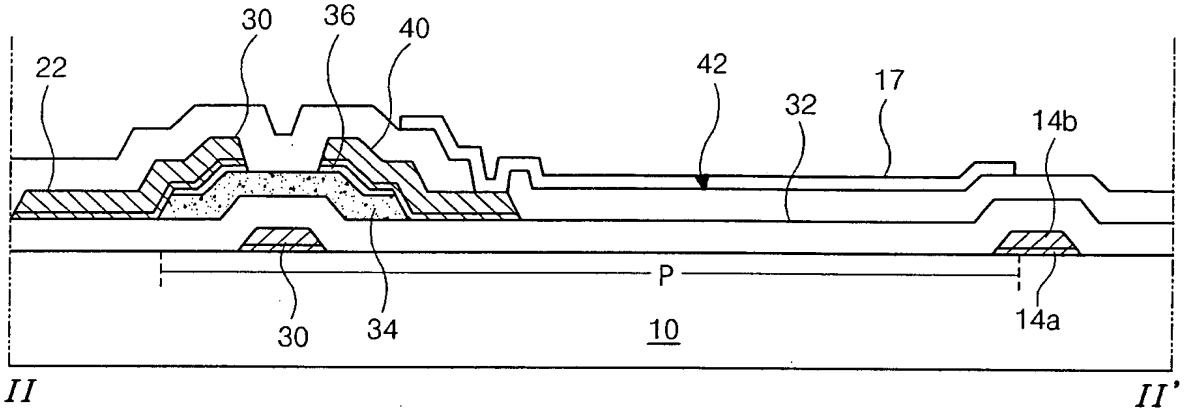
The method according to claim 3, wherein the pixel electrode includes one of a transparent conductive metallic material having indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

[DRAWINGS]

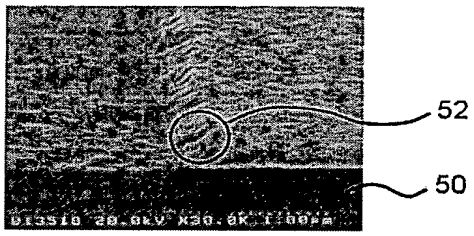
[Fig. 1]



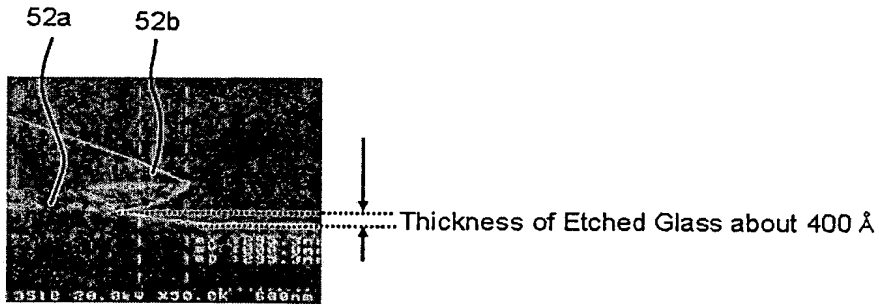
[Fig. 2]



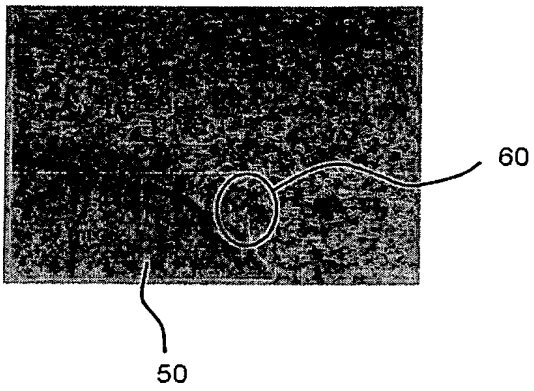
[Fig. 3]



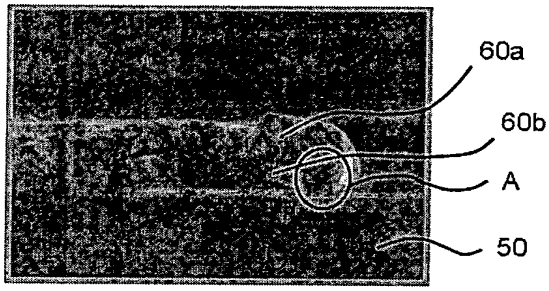
[Fig. 4]



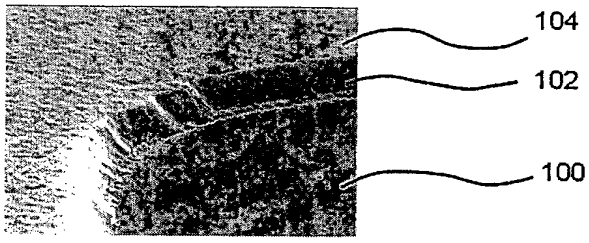
[Fig. 5]



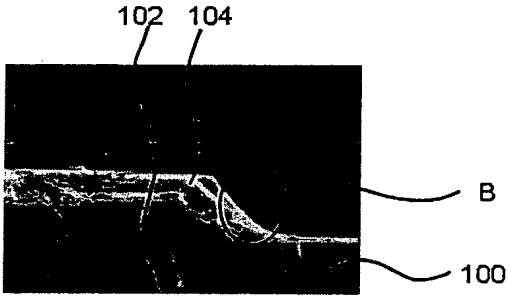
[Fig. 6]



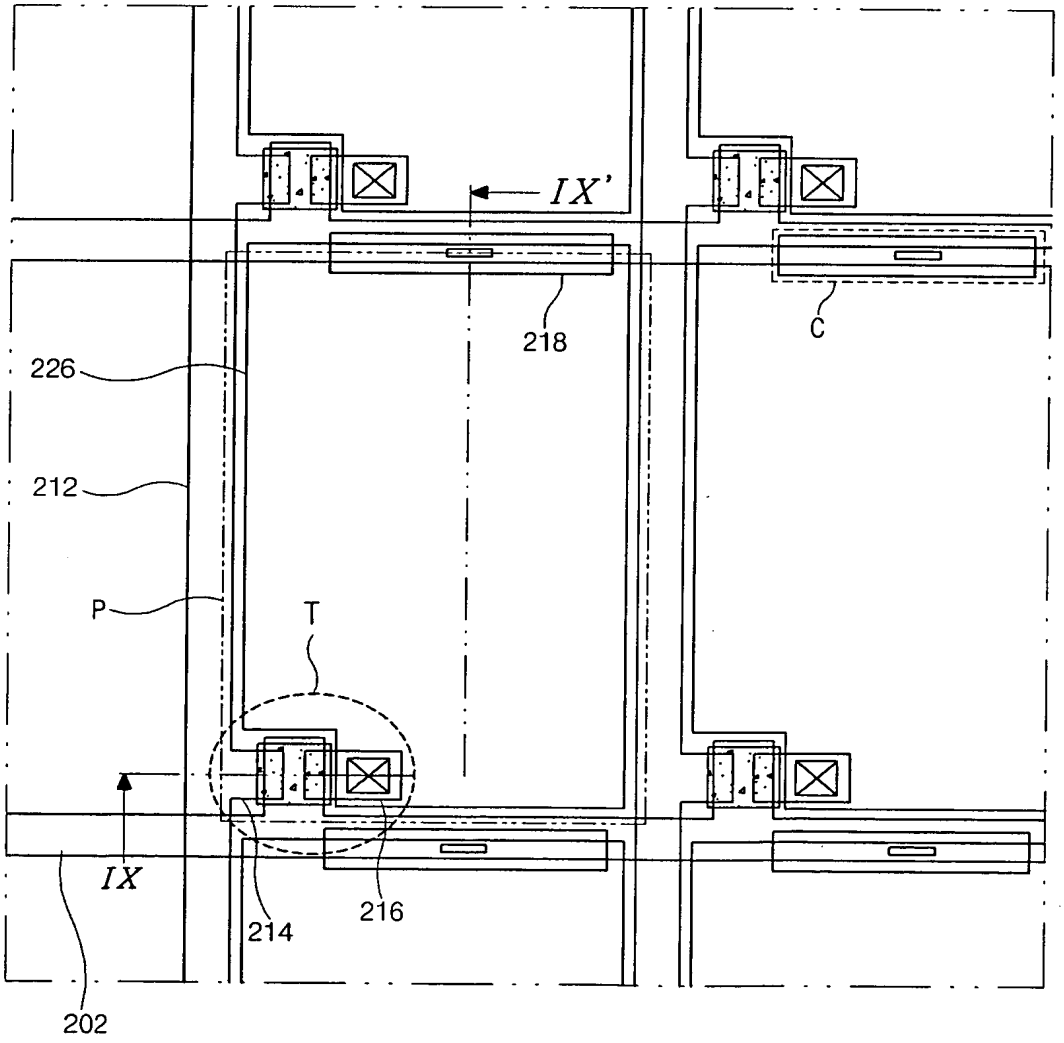
[Fig. 7]



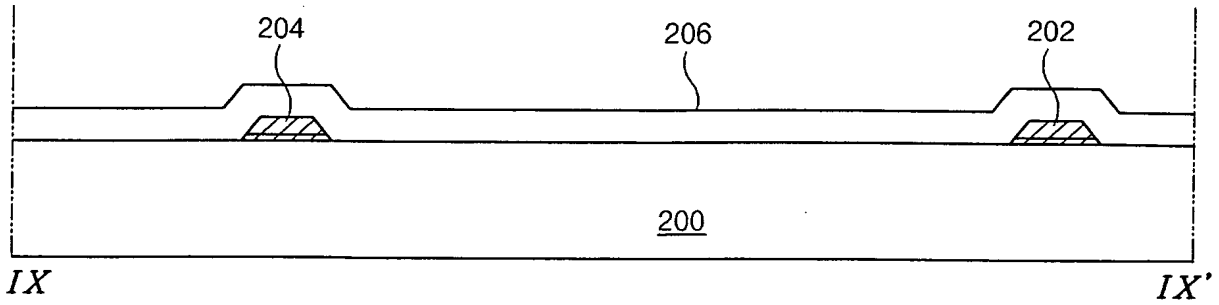
[Fig. 8]



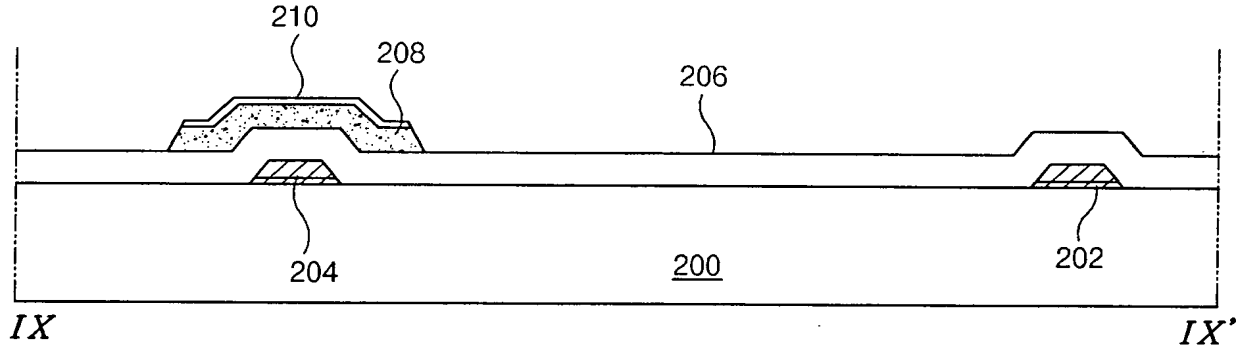
[Fig. 9]



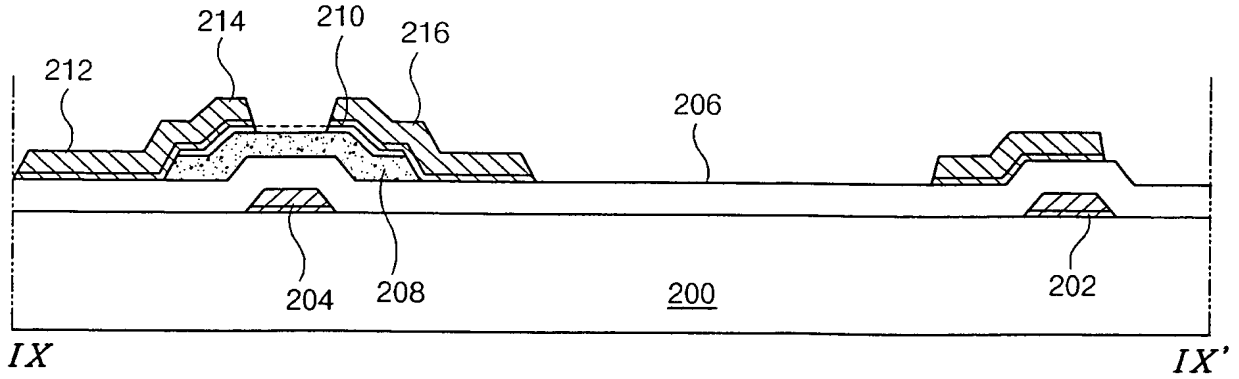
[Fig. 10a]



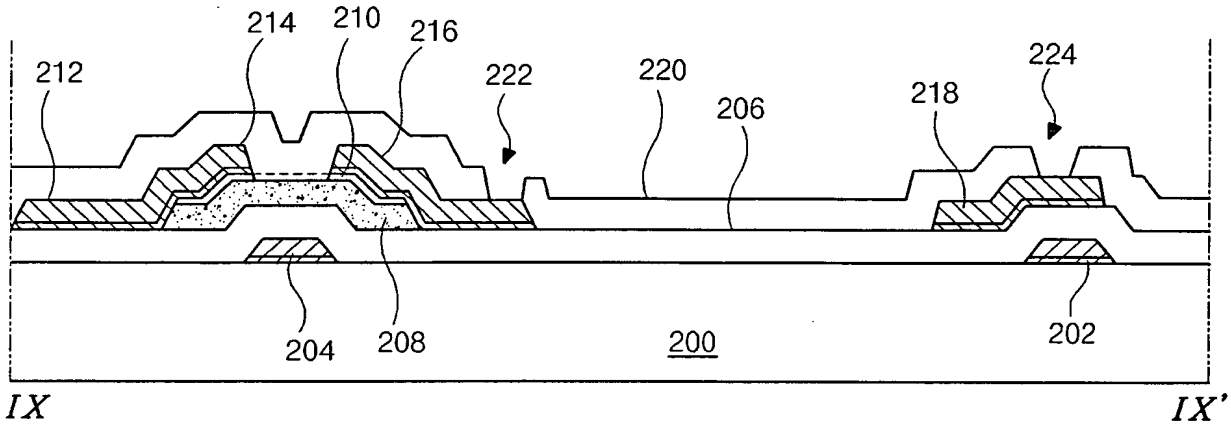
[Fig. 10b]



[Fig. 10c]



[Fig. 10d]



[Fig. 10e]